INCH-POUND

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MILITARY SPECIFICATION

DELAY LINES, PASSIVE, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for fixed passive (tapped and untapped) pulse delay lines.

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). The term Part or Identifying Number (PIN) is equivalent to the term Part Number which was previously used in this specification. The PIN is as shown in the following example:

M	83531	/01	-001
Military designator	Specification number	Specification sheet number (two digits)	Dash number (see 3.1)

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: 645 LOG/ES, Gentile Station, 1060 Hamilton Street, Dayton, OH 45444-5400 by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5999

SPECIFICATIONS

FEDERAL

J-W-1177	-	Wire, Magnet, Electrical.
QQ-S-571	-	Solder, Tin Alloy; Tin-Lead Alloy; and Lead Alloy.

MILITARY

MIL-F-14256	-	Flux, Soldering, Liquid (Rosin Base).
MIL-S-19491	-	Semiconductor Device, Packaging of.
MIL-R-55342	-	Resistor, Fixed, Film, Chip, Established Reliability, General Specification For.
MIL-C-55681	-	Capacitor, Chip, Multiple Layer, Fixed, Unencapsulated, Ceramic Dielectric, Established Reliability, General Specification For.
MIL-D-83531/1	-	Delay Lines, 10-Tap, Dual-In-Line, 14-Pin.

STANDARDS

MILITARY

MIL-STD-202	-	Test Methods for Electronic and Electrical Component Parts.
MIL-STD-454	-	Standard General Requirements for Electronic Equipment.
MIL-STD-790	-	Product Assurance Program for Electronic and Fiber Optic Parts Specifications.
MIL-STD-810	-	Environmental Test Methods and Engineering Guidelines.
MIL-STD-1276	-	Leads for Electronic Component Parts.
MIL-STD-1285	-	Marking of Electrical and Electronic Parts.
MIL-STD-45662	-	Calibration Systems Requirements.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

EIA-RS-242	-	Definitions for Electromagnetic Delay Lines.
EIA-557	-	Statistical Process Control Systems.

(Application for copies should be addressed to the Electronic Industries Association Engineering Office, 11 West 42nd Street, New York, NY 10036.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. Delay lines furnished under this specification shall be products which are authorized by the qualifying activity for listing on the applicable qualified products list at the time of award of contract (see 6.4 and table I). In addition, the manufacturer shall certify in writing that the product assurance requirements of 3.3 have been met and are being maintained.

3.3 Product assurance requirements. Delay lines shall be subjected to and passed all applicable requirements, tests, and inspections detailed herein, including qualification and quality conformance inspection requirements and the product assurance program. A product assurance program for delay lines furnished under this specification shall be established and maintained in accordance with the procedures and requirements specified in MIL-STD-790.

3.3.1 Statistical Process Control (SPC). The contractor shall implement and use SPC techniques in the manufacturing process for parts covered by this specification. The SPC program shall be developed and maintained in accordance with EIA-557 or an equivalent specification as approved by DESC-EMM. The program shall be documented and maintained as part of the overall reliability assurance program as specified in MIL-STD-790. The implementation date for SPC shall be no later than 12 months from the date of revision A to this specification. Processes for application of SPC techniques shall include, but are not limited to:

a. Chip capacitor inspection and test (after attachment).

b. Pre-assembly coil inspection and test.

c. Finishing: Inspection after post mold cleaning and before stamping and final assembly operations, test, and inspection.

3.4 Materials. The materials shall be as specified herein; however, when a definite material is not specified, a material shall be used which will enable the delay lines to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product (see 4.6.1).

3.4.1 Flammable materials. Materials used in the construction of delay lines shall be nonflammable and nonexplosive.

3.4.2 Corrosive materials. Corrosive materials used in any of the manufacturing processes shall be removed or neutralized so that no corrosion of delay lines will result from such use. Materials used in the construction of delay lines shall be noncorrosive.

3.4.3 Solder and soldering flux. Solder shall be in accordance with QQ-S-571. Soldering flux shall be in accordance with MIL-F-14256.

3.4.4 Case material. Unless otherwise specified (see 3.1), cases may be of metallic or nonmetallic material. All metallic surfaces shall be protected against corrosion by a suitable finish and shall be free from blisters and other defects which may affect the protective properties of this finish.

3.4.5 Terminals. Terminals shall be type LR(0.52) G-**-C* in accordance with MIL-STD-1276. The use of pure tin plating as an undercoat or final finish is prohibited effective 6 months from the date of revision A to MIL-D-83531 (see 6.5).

3.4.5.1 Solder dip (retinning leads). Only the manufacturer (or his authorized category B or C distributor) may solder dip/retin the leads of products supplied to this specification, provided the solder dip process has been approved by the qualifying activity.

TABLE I. Qualification inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units	Number of allowable failures
Group I				
Dimensions	3.5.1	4.6.2		
Thermal shock (50 cycles)	3.6	4.6.4		
Seal	3.7	4.6.5	22	2
Electrical characteristics	3.8	4.6.6		
Visual inspection 1/	3.5.2	4.6.3		
Group II				
Moisture resistance	3.11	4.6.9		
Salt spray (corrosion) (metal cases only)	3.12	4.6.10	6	0
Vibration	3.13	4.6.11		
Shock	3.14	4.6.12		
Electrical characteristics	3.8	4.6.6		
Visual inspection 1/	3.5.2	4.6.3		
Group III				
Thermal shock (50 cycles)	3.6	4.6.4		
Life	3.15	4.6.13		
Terminal strength	3.16	4.6.14		
Fungus 2/	3.17	4.6.15	6	0
Electrical characteristics	3.8	4.6.6		
Dielectric withstanding voltage at reduced barometric pressure	3.18	4.6.16		
Visual inspection 1/	3.5.2	4.6.3		
Group IV				
Resistance to soldering heat	3.19	4.6.17	4	0
Flammability	3.20	4.6.18		
Group V				
Resistance to solvents	3.9	4.6.7	4	0
Solderability	3.10	4.6.8		

1/ The "JAN" or "J" marking and PIN are not required on qualification samples.

2/ The fungus test need not be performed if the manufacturer provides certification that all external materials are nonnutrient to fungus growth or suitably treated to retard fungus growth.

3.4.5.1.1 Qualifying activity approval. Approval of the solder dip process will be based on one of the following options:

a. When the original lead finish qualified was hot-solder dip lead finish 52 of MIL-STD-1276 (Note: The 200 microinch maximum thickness requirement is not applicable), the manufacturer shall use the same solder dip process for retinning as was used in the original manufacture of the products.

b. When the lead originally qualified was not hot-solder dip lead finish 52 of MIL-STD-1276, approval for the process to be used for solder dip shall be based on the following test procedure:

(1) Thirty samples of any PIN for each style and lead finish shall be subjected to the manufacturer's solder dip process. Following this process, the delay lines shall be subjected to the electrical tests of the group A inspection, with no defects allowed.

(2) Ten of the 30 samples shall then be subjected to the solderability test as specified in 4.6.8. No defects are allowed.

3.4.5.1.2 Solder dip/retinning options. The manufacturer (or his authorized category B or C distributor) may solder dip/retin as follows:

a. After the solder dip/retinning process, the electrical measurements required in the group A inspection shall be performed on 100 percent of the lot. The maximum Percent Defective Allowable (PDA) for the electrical measurements shall be 10 percent (or one device, whichever is greater). Failed lots may be re-dipped or re-tinned, then subjected to the electrical measurements specified in group A. Failed lots may be reinspected one time only. The maximum PDA for reinspected lots shall be 7 percent. In all circumstances, group A inspection in accordance with table II shall be performed.

b. As a corrective action if the lot fails the group A solderability test, the procedure described in 3.4.5.1.1a may be performed.

3.4.5.2 Meniscus. Terminals shall be free of case meniscus or other foreign material and shall be solderable for a minimum of .010 inch (0.25 mm) above the seating plane of the delay line.

3.4.6 Passive circuit elements. Capacitors shall be qualified or screened to MIL-C-55681. Resistors shall be qualified or screened to MIL-R-55342. Inductors shall be so designed as to allow the delay line to meet the requirements specified herein.

3.4.7 Magnet wire. Magnet wire shall be in accordance with J-W-1177.

3.4.8 Electronic components. Electronic components shall be selected in accordance with the applicable requirements of MIL-STD-454. Delay lines shall meet the performance requirements and product characteristics specified herein. After qualification, any changes in parts or materials shall be submitted to the Government qualifying activity for approval.

3.5 Design and construction. Delay lines shall be of the design, construction, and physical dimensions specified in the applicable specification sheet (see 3.1).

3.5.1 Dimensions. When delay lines are inspected in accordance with 4.6.2, the dimensions shall be within the tolerances specified on the applicable specification sheet (see 3.1).

3.5.2 Visual inspection. When delay lines are inspected in accordance with 4.6.3, they shall not exhibit flaking, pitting, blistering, peeling, cracks, bursting, bulging, or other visual defects. The delay lines shall also meet the requirements of 3.1, 3.22, and 3.23.

3.6 Thermal shock. When delay lines are tested as specified in 4.6.4, not more than 10 percent of the surface shall have peeling, flaking, chipping, cracking, or other impairment of the protective finish. There shall be no evidence of other physical damage such as cracks, bursting, or bulging of the case or other defects that would affect the mechanical or electrical operation. There shall be no electrical discontinuity.

3.7 Seal. When delay lines are tested as specified in 4.6.5 there shall be no evidence of continuous air bubble flow or compound leakage.

3.8 Electrical characteristics. Delay lines shall be capable of meeting all the electrical requirements specified (see 3.1 and 3.8.1 through 3.8.8).

3.8.1 Delay time. When tested in accordance with 4.6.6.1.1, the overall specified delay time of the line shall be as specified. The input-to-tap and tap-to-sequential tap shall be as specified (see 3.1).

3.8.2 Rise time. When measured in accordance with 4.6.6.1.2, the rise time of pulses taken at the point of maximum delay shall not exceed the value specified (see 3.1). The rise time measured at the taps shall not exceed the rise time required at the point of maximum delay.

3.8.3 Voltage attenuation. When measured in accordance with 4.6.6.1.3, the voltage attenuation of pulses taken at the point of maximum delay with respect to the input pulse amplitude shall not exceed the value specified (see 3.1). The voltage attenuation measured at the taps shall not exceed the voltage attenuation required at the point of maximum delay.

3.8.4 Distortion. Unless otherwise specified (see 3.1), when measured in accordance with 4.6.6.1.4, the all encompassing distortion of pulses appearing at the point of maximum delay shall not exceed ±15 percent.

3.8.5 Delay time variation with temperature. When tested in accordance with 4.6.6.1.5, the delay time variation with temperature shall not exceed the value specified (see 3.1).

3.8.6 DC resistance. When delay lines are tested as specified in 4.6.6.1.6, the dc resistance shall be as specified (see 3.1).

3.8.7 Nominal characteristic impedance. When tested in accordance with 4.6.6.1.7, nominal characteristic impedance shall be as specified on individual specification sheets (see 3.1).

3.8.8 Insulation resistance. Unless otherwise specified (see 3.1), when delay lines are tested in accordance with 4.6.6.1.8, the minimum insulation resistance shall be 1,000 megohms (MΩ).

3.9 Resistance to solvents. When delay lines are tested as specified in 4.6.7, there shall be no evidence of mechanical damage and all markings shall remain legible. The paint or exterior finish shall not soften, peel, or show other signs of deterioration.

3.10 Solderability. When delay lines are tested as specified in 4.6.8, they shall meet the applicable criteria for terminal evaluation in the test method.

3.11 Moisture resistance. When tested in accordance with 4.6.9, there shall be no evidence of physical damage that would affect the mechanical or electrical operation of the delay line. There shall be no evidence of electrical discontinuity.

3.12 Salt spray (corrosion) (metal cases only) (when specified, see 3.1). When delay lines are tested as specified in 4.6.10, there shall be no evidence of corrosion as exhibited by any visible degradation of the surfaces that can be attributed to flaking, pitting, blistering, or otherwise loosened protective coating or metal surface.

3.13 Vibration. When delay lines are tested as specified in 4.6.11, there shall be no leakage of filling material and no evidence of other physical damage such as cracks, bursting, or bulging of the case. There shall be no evidence of mechanical damage and there shall be no electrical discontinuity during the test.

3.14 Shock. When delay lines are tested as specified in 4.6.12, there shall be no leakage of filling material and no evidence of other physical damage such as cracks, bursting, or bulging of the case. There shall be no evidence of mechanical damage and there shall be no electrical discontinuity during the test.

3.15 Life. When delay lines are tested as specified in 4.6.13, there shall be no evidence of impairment to the protective finish or of other physical damage such as cracks, bursting, or bulging of the case. There shall be no evidence of electrical discontinuity during the test.

3.16 Terminal strength. When delay lines are tested as specified in 4.6.14, there shall be no evidence of loosening, rupturing, or other mechanical damage. Bends shall not be considered as damage unless surface cracking is evident. There shall be no rotation of the terminals. Rotation of the external portion of the metallic portion of a "hook" type terminal exceeding 10 degrees shall constitute a failure.

3.17 Fungus. The manufacturer shall certify that all external materials are nonnutrient to fungus growth or are suitably treated to retard fungus growth, or shall perform the test specified in 4.6.15. When delay lines are tested, there shall be no evidence of fungus growth on the external surfaces.

3.18 Dielectric withstanding voltage at reduced barometric pressure. When delay lines are tested as specified in 4.6.16, there shall be no arcing, flashover, breakdown of insulation, or other evidence of damage.

3.19 Resistance to soldering heat. When delay lines are tested as specified in 4.6.17, there shall be no softening of the insulation or loosening of the windings or terminals, no evidence of internal solder reflow or heat damage, and no evidence of discontinuity.

3.20 Flammability. When delay lines are tested as specified in 4.6.18, there shall be no evidence of violent burning which results in an explosive-type fire, and the coating material used shall be self-extinguishing. Delay lines shall not be considered to have failed if they are consumed by the applied flame. Delay lines shall be considered to have failed only if an explosion or dripping of flaming material occurs, an explosive-type flame is produced, or if visible burning continues beyond the allowable duration of 3 minutes after removal of the applied flame.

3.21 Winding continuity. When delay lines are tested as specified in 4.6.19, all windings shall be electrically continuous.

3.22 Marking.

3.22.1 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN and "J", to indicate that items so marked or identified are manufactured to, and meet all the requirements of military specifications. Accordingly, items acquired to and meeting all the criteria specified herein and in applicable detail specifications shall bear the certification mark "JAN", except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the PIN, except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the PIN. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable detail specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets or detail specifications, the manufacturer shall remove the "JAN" or the "J" from the sample tested and also from all items represented by the sample. The "JAN" or "J" certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration No. 504,860 for the certification mark "JAN".

3.22.2 Full marking. Each delay line shall be marked on the top in accordance with method I of MIL-STD-1285 with the following information:

a. "JAN" or "J" marking (see 3.22.1).

b. Military PIN (see 1.2.1).

c. Index mark identification (next to pin 1, input) (see 3.1).

d. Manufacturer's CAGE code or logo.

e. Date code.

3.23 Workmanship. Delay lines shall be processed in such a manner as to be uniform in quality and shall be free from defects that would affect their performance, life, or serviceability. Parts shall be free of flash pits, voids, and excessive mold marks. A visible parting line is acceptable.

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. Unless otherwise specified in the acquisition document, the contractor is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the acquisition document, the contractor may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure materials and procedures conform to prescribed requirements.

4.1.1 Responsibility for compliance. Delay lines shall meet all the requirements of sections 3 and 5 herein. The inspections set forth in this specification shall become a part of the contractor's overall inspection system or quality program. The absence of any inspection requirements in the specification shall not relieve the contractor of the responsibility of assuring that all products or supplies submitted to the Government for acceptance comply with all requirements of the contract. Sampling in quality conformance does not authorize submission of known defective material, either indicated or actual, nor does it commit the Government to acceptance of defective material.

4.1.2 Test equipment and inspection facilities. Test and measuring equipment and inspection facilities of sufficient accuracy, quality, and quantity to permit performance of the required inspections shall be established and maintained by the manufacturer. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with MIL-STD-45662.

4.1.3 Product assurance program. A product assurance program shall be established and maintained in accordance with 3.3.

4.2 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Quality conformance inspection (see 4.5).

4.3 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the "general requirements" section of MIL-STD-202.

4.3.1 Reference test circuit, test equipment, and measurements. Reference test circuit, test equipment, and measurements shall be as specified in 4.3.1.1 through 4.3.1.6. Any equivalent test circuit may be used. In case of conflict, the reference test circuit contained herein shall take precedence.

4.3.1.1 Reference test circuit. The reference test circuit shall be as shown on figure 1. The pulse generator shall be loaded with an L pad to match delay line impedance to generator. The delay line shall be terminated in the nominal terminating impedance within ±1 percent. The test circuit capacitances, including probe, shall not exceed 3 picofarads (pF). Waveform characteristics are shown on figure 2.

4.3.1.2 Test equipment. The test equipment shall be as follows:

a. Marker generator: Tektronix type TG501, type 2901, or equivalent.

b. Pulse generator: Capable of 1 nanosecond (ns) rise time when measuring time, and 5 ns when measuring distortion.

c. Oscilloscope: 350 megahertz (MHz) bandwidth minimum, analog, dual channel.

d. Probe: The oscilloscope's recommended probe should be used. The probe capacitance and circuit capacitance shall be 3 pF maximum at probe tip. The probe impedance shall be 10 times the impedance of the device being measured, minimum.

e. Test fixture: A fixture with a massive ground plane shall be used. All lead lengths shall be .25 inch (6.4 mm) maximum. Stray capacitance and inductance shall be kept below 3 pF and 10 nanohenrys (nh), respectively. Resistors shall be noninductive types. Coaxial cables, RG-58 c/u or equivalent, 18 inches length maximum, shall be used.

4.3.1.3 Delay measurements. The basic steps for measurement of delay shall be as follows:

a. Establish reference $t_d = 0$.

b. Sweep speed: Use sweep speed such that the output rise is displayed across 4 centimeters (cm) minimum so that it crosses the screen at approximately 45 degrees. The markers may then be chosen so as to provide a mark each 1 to 2 cm.

c. Display markers selected (b. above) on channel B.

d. Display input pulse on channel A. Set amplitude deflection for 100 percent (4 cm minimum).

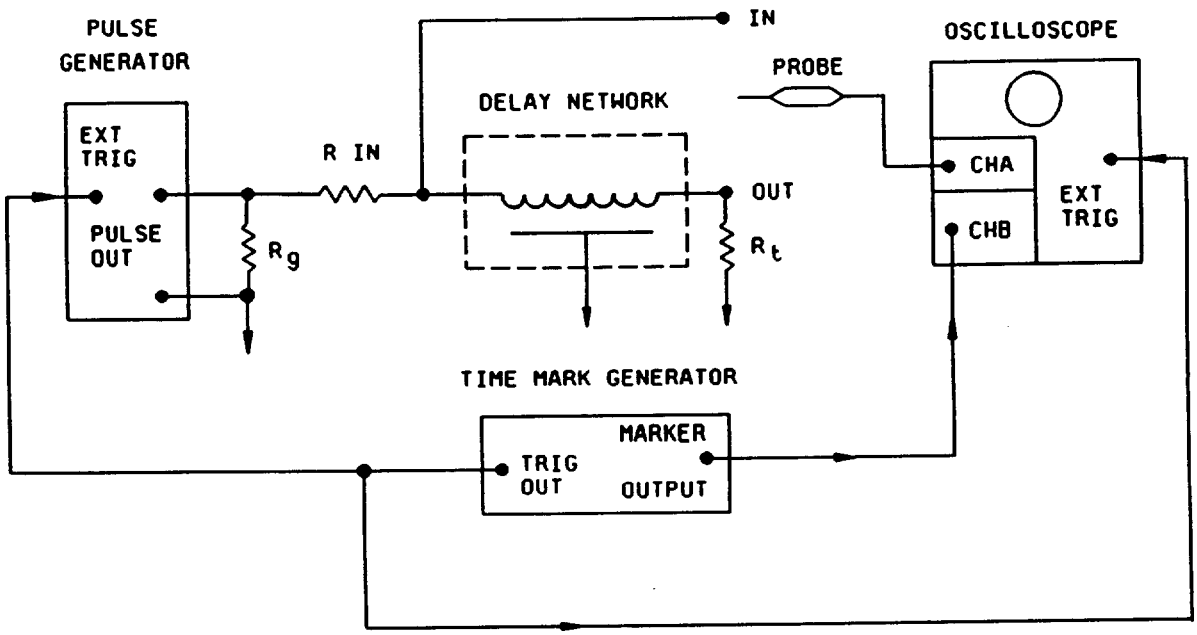
e. Adjust "pulse position vernier" on pulse generator for coincidence of 50 percent amplitude ($.5E_i$) point of input pulse and a reference marker.

f. To measure delay of output pulse, move channel A probe to output test point.

g. Adjust delay time on oscilloscope, counting markers, until the output pulse is displayed.

h. Adjust amplitude deflection on channel A to 100 percent (4 cm minimum).

i. Delay equals the number of markers plus increment between last marker and 50-percent point ($.5E_o$) of output pulse.



NOTE: All measurements refer to definitions contained in EIA Standard RS-242.
R IN = Input matching resistance.
R_g = Generator terminating impedance.
R_t = Terminating resistance.

FIGURE 1. Reference test circuit.

Nominal terminating impedance ±1%	R in ±5%	R_a ±5%
50Ω see note	25.0	50.0
100Ω	70.7	70.7
200Ω	173.2	57.7
250Ω		
300Ω		
350Ω	324.0	54.0
360Ω	334.1	53.9
400Ω		
500Ω	474.3	52.7

NOTE: No pad used when terminating impedance is 50Ω.

FIGURE 1. Reference test circuit - Continued.

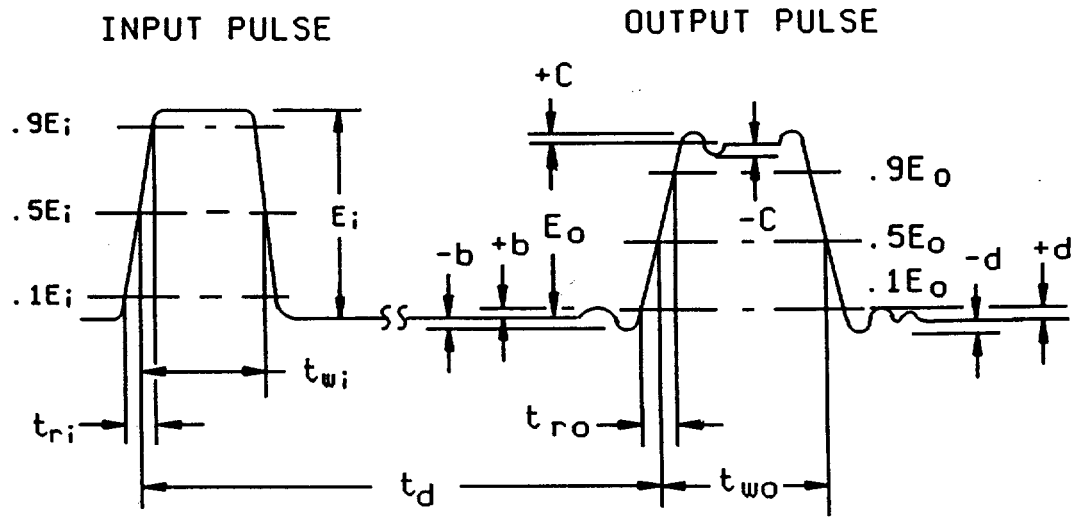


FIGURE 2. Waveform characteristics.

4.3.1.4 Rise time measurements. Rise time measurements shall be made as follows:

a. Set sweep speed such that the output rise is displayed across 4 cm minimum so that it crosses the screen at approximately 45 degrees. The markers may then be chosen so as to provide a mark approximately 1/10 the rise time being measured or 1 ns, whichever is greater.

b. Display markers selected (a. above) on channel B.

c. Display input pulse (input test point) on channel A. Set amplitude deflection for 100 percent (4 cm minimum).

d. Adjust input pulse rise time (t_{ri}) after replacing the delay line with a direct short between the input and output terminals. The shorting wire should be as short as possible. Measure at test fixture input.

e. Remove short and reinstall delay line. Measure output rise time by moving channel A probe to output test point.

f. Adjust delay time on oscilloscope until the output pulse is displayed.

g. Adjust amplitude deflection on channel A to 100 percent (4 cm minimum).

h. Measure output pulse rise time (t_{ro}) (from point $.1E_o$ to $.9E_o$).

i. If another method of measuring rise time is used, the following formula may apply:

$$\text{True rise time} = \sqrt{t_{ro}^2 - t_{ri}^2}$$

4.3.1.5 Distortion measurements. Distortion measurements shall be made as follows:

a. Display entire output pulse width using 4 cm minimum of oscilloscope screen. Adjust amplitude deflection on channel A for 100 percent (4 cm minimum) deflection.

b. Measure amplitudes of output pulse distortion b, c, and d (see RS-242).

c. Calculate delay line output pulse distortion (So)b, (So)c, (So)d using worst case conditions (see RS-242).

$$(So)b\% = \frac{|b|}{E} \times 100 \qquad (So)c\% = \frac{|c|}{E} \times 100 \qquad (So)d\% = \frac{|d|}{E} \times 100$$

4.3.1.6 Voltage attenuation measurements. Voltage attenuation measurements shall be made as follows:

a. Connect a short between the "in" and "out" points shown on figure 1.

b. Adjust scope to display input pulse amplitude as for delay time. Measure input pulse amplitude (E_i) at input test point.

c. Remove short and replace with the delay line under test.

d. Move probe to output test point.

e. Adjust delay time on oscilloscope to display output pulse.

f. Measure output pulse amplitude (E_o).

g. Calculate attenuation (see RS-242).

$$\text{Voltage attenuation} = \frac{E_i - E_o}{E_i} \times 100$$

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.4) on sample units produced with equipment and procedures normally used in production.

4.4.1 Sample. The number of units comprising a sample of delay lines to be submitted for qualification inspection shall be as specified in table I and the appendix.

4.4.2 Test routine. Qualification samples shall be subjected to the tests of table I, in the order shown. All sample units shall be subjected to the tests of group I. The sample delay lines shall then be further divided into four groups (see table I). The tests within each group shall be performed in the order shown.

4.4.3 Failures. Failures in excess of those allowed in table I shall be cause for refusal to grant qualification.

4.4.4 Retention of qualification. To retain qualification, the contractor shall forward a report at least every 12 months to the qualifying activity. The qualifying activity shall establish the reporting date. The report shall consist of:

a. A summary of the results of the tests performed for the group A inspection indicating, as a minimum, the number of lots that have passed and the number that have failed. The results of tests of all reworked lots shall be identified and accounted for. Failure to submit this report within 30 days after the end of each reporting period may result in loss of qualification.

b. In the event that no production occurred during the 12-month reporting period, a report shall be submitted certifying that the company still has the capabilities and facilities necessary to produce the item. If during two consecutive reporting periods there has been no production, the manufacturer may be required, at the discretion of the qualifying activity, to submit the products (a representative sample of each delay line) to testing in accordance with the qualification inspection requirements. In addition to the above, the manufacturer shall requalify every 36 months (see 4.5.2). Actual group A test data shall be submitted to the qualifying activity upon request. The manufacturer shall immediately notify the qualifying activity if any failures occur during requalification.

c. A summary of written reports based on the required program covering analyses of failures other than those reported by equipment contractors shall be submitted along with regularly scheduled retention of qualification reports.

4.5 Quality conformance inspection and in-process inspection.

4.5.1 Inspection of product for delivery. Inspection of product for delivery shall consist of the group A inspection.

4.5.1.1 Production and inspection lots.

4.5.1.1.1 Production lot. A production lot shall consist of all delay lines of a single PIN produced under essentially the same conditions, and offered for inspection at one time.

4.5.1.1.2 Inspection lot. An inspection shall consist of all delay lines of the same specification sheet manufactured under the same processes and conditions during a manufacturing period of one month maximum.

4.5.1.2 Group A inspection. Group A inspection shall consist of the inspections specified in table II, in the order shown.

4.5.1.2.1 Sampling plan.

4.5.1.2.1.1 Subgroup I. One hundred percent inspection shall be performed on a production lot basis as specified in table II. Lots having more than five percent total rejects shall not be furnished on the contract. Delay lines out of specification limits shall not be shipped with the lot.

TABLE II. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph
Subgroup I		
Thermal shock (15 cycles)	3.6	4.6.4
Seal	3.7	4.6.5
Delay time (all taps and output)	3.8.1	4.6.6.1.1
Rise time (output only)	3.8.2	4.6.6.1.2
Distortion (output only)	3.8.4	4.6.6.1.4
Insulation resistance	3.8.8	4.6.6.1.8
Subgroup II		
Dimensions	3.5.1	4.6.2
Visual inspection	3.5.2	4.6.3
DC resistance	3.8.6	4.6.6.1.6
Voltage attenuation (output only)	3.8.3	4.6.6.1.3
Delay time variation with temperature (output only)	3.8.5	4.6.6.1.5
Nominal characteristic impedance (at input)	3.8.7	4.6.6.1.7
Subgroup III		
Solderability	3.10	4.6.8

4.5.1.2.1.2 Subgroup II. A sample of parts shall be randomly selected from each production lot in accordance with table III. If one or more defects are found, the lot shall be rescreened and the defective parts removed. After screening and removal of defective parts, a new sample of parts shall be randomly selected in accordance with table III. If one or more defects are found in the second sample, the lot shall be rejected and shall not be supplied to this specification.

TABLE III. Sampling plan for subgroup II of group A inspection. 1/

Lot size	Sample size
1 to 13	All
14 to 150	13
151 to 280	20
281 to 500	29
501 to 1,200	34
1,201 to 3,200	42
3,201 to 10,000	50
10,001 to 35,000	60
35,001 to 150,000	74
150,001 to 500,000	90
500,001 and over	102

1/ No defects are allowed.

4.5.1.2.1.3 Subgroup III. Five samples shall be randomly selected from each inspection lot and subjected to the solderability test. The manufacturer may use electrical rejects from the subgroup I screening tests for all or part of the samples to be used for solderability testing. If there are one or more defects, the lot shall have failed.

4.5.1.2.1.3.1 Failed lots. Failed lots may be reworked using the following procedure: The manufacturer submits the failed lot to a 100 percent solder dip using the process described in 3.4.5.1. Following the solder dip, the seal test and electrical measurements required in group A, subgroup I, shall be repeated on 100 percent of the lot. The PDA for the electrical measurements shall be as for the subgroup I tests. Five additional samples shall then be selected and subjected to the solderability test with zero defects allowed. If the lot fails this solderability test, it may be reworked a second time and retested. If the lot fails the second rework it shall be rejected and shall not be furnished to this specification.

4.5.1.2.1.3.2 Solderability test samples. The solderability test is considered to be destructive due to the steam aging process involved in the test. Samples submitted to this test shall not be supplied on the contract.

4.5.1.2.2 Disposition of sample units. Sample units which have passed all the group A inspections shall be delivered on the contract or purchase order if the lot is accepted. (Exception: Parts which have undergone solderability testing shall not be delivered; see 4.5.1.2.1.3.)

4.5.2 Requalification inspection. Every 36 months, the requalification inspection shall be performed at a laboratory acceptable to the government (see 6.4) on sample units produced with equipment and procedures used in production. Requalification inspection shall consist of the inspections specified in table IV, in the order shown.

4.5.2.1 Sample. The number of sample units shall be as specified in table IV.

4.5.2.2 Failures. Failures in excess of those allowed in table IV shall be cause for the entire sample lot to fail.

4.5.2.3 Disposition of sample units. Sample units which have been subjected to requalification inspection shall not be delivered on the contract or purchase order.

4.5.2.4 Noncompliance. If a sample fails to pass the requalification inspection, the manufacturer shall immediately notify the qualifying activity and the cognizant inspection activity of the cause of such failure and take corrective action on the materials and/or processes, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials, processes, ect., and which were subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action acceptable to the qualifying activity has been taken. After corrective action has been taken, the requalification inspection shall be repeated on additional sample units (all inspections, or the inspection which the original sample failed, at the option of the qualifying activity). Group A inspection may be reinstituted; however, final acceptance and shipment shall be withheld until the requalification inspection has shown that the corrective action was successful. In the even of a failure after reinspection, the cause of such failure shall be immediately furnished to the cognizant inspection activity and the qualifying activity.

4.5.3 Inspection of packaging. The sampling and inspection of the preservation, packing, and container marking shall be in accordance with the requirements for semiconductor devices in MIL-S-19491.

TABLE IV. Requalification inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units	Number of allowable failures
Group I				
Dimensions	3.5.1	4.6.2		
Thermal shock (50 cycles)	3.6	4.6.4		
Seal	3.7	4.6.5	14	2
Electrical characteristics	3.8	4.6.6		
Visual inspection	3.5.2	4.6.3		
Group II				
Resistance to solvents	3.9	4.6.7		
Solderability	3.10	4.6.8		
Moisture resistance	3.11	4.6.9		
Salt spray (corrosion) (metal cases only)	3.12	4.6.10	4	0
Vibration	3.13	4.6.11		
Shock	3.14	4.6.12		
Electrical characteristics	3.8	4.6.6		
Visual inspection	3.5.2	4.6.3		
Group III				
Life	3.15	4.6.13		
Terminal strength	3.16	4.6.14		
Fungus 1/	3.17	4.6.15	4	0
Electrical characteristics	3.8	4.6.6		
Dielectric withstanding voltage at reduced barometric pressure	3.18	4.6.16		
Visual inspection	3.5.2	4.6.3		
Group IV				
Resistance to soldering heat	3.19	4.6.17	4	0
Flammability	3.20	4.6.18		

1/ The fungus test need not be performed if the manufacturer provides certification that all external materials are nonnutrient to fungus growth or suitably treated to retard fungus growth.

4.6 Methods of inspection.

4.6.1 Materials. The manufacturers shall certify in writing that the materials used meet all the requirements of 3.4.

4.6.2 Dimensions. All dimensions shall be measured with a suitable instrument (see 4.1.2) to the requirements of 3.5.1.

4.6.3 Visual inspection. Delay lines shall be visually inspected with normal or corrected 20/20 vision to meet the requirements of 3.5.2.

4.6.4 Thermal shock (see 3.6). Unless otherwise specified (see 3.1), delay lines shall be tested in accordance with method 107 of MIL-STD-202. Measurement before and after: Winding continuity in accordance with 3.21 and 4.6.19.

a. Test condition B for group A. (Exception: Low temperature shall be -55°C (+0/-3°C) and 15 cycles shall be used.)

b. Test condition B-2 (50 cycles) for qualification, except low temperature shall be -55°C (+0/-3°C).

4.6.5 Seal (see 3.7). Delay lines shall be immersed in a bath of water (or any other liquid of no greater density and surface tension) and maintained at a temperature of at least 85°C for 2 to 3 minutes. Prior to immersion, delay lines shall reside in an ambient temperature of less than 40°C for a minimum of 15 minutes. The temperature of the delay lines shall not exceed 40°C at the time of immersion. Delay lines shall be arranged in a single layer to allow visible access to all tested units.

4.6.6 Electrical characteristics (see 3.8).

4.6.6.1 Pulse methods. The delay time, rise time, attenuation, distortion, and thermal stability tests shall be conducted by applying an input pulse with a rise time of 1 ns to 5 ns to the delay line. The terminating impedance of the delay line shall be resistive and within ±1 percent of the value specified. Unless otherwise specified (see 3.1), the source impedance shall be within ±5 percent of the value of the terminating impedance.

4.6.6.1.1 Delay time. The time delay of pulses taken at each tap and the output of delay lines shall be measured to determine conformance with 3.8.1. In the case of sectionalized lines, the time delay of any combination of tandem sections shall be measured.

4.6.6.1.2 Rise time. The rise time of pulses taken at the output terminals (for sectionalized lines with all sections in tandem), shall be measured to determine conformance with 3.8.2.

4.6.6.1.3 Voltage attenuation. The amplitude of pulses taken at the input and output terminals (for sectionalized lines with all sections in tandem), shall be measured and the attenuation computed (see 3.8.3).

4.6.6.1.4 Distortion. The distortion of pulses taken at the output terminals (for sectionalized lines with all sections in tandem), when the delay line is fed with the specified input pulses shall be measured to determine conformance with 3.8.4.

4.6.6.1.5 Delay time variation with temperature. The delay line shall be enclosed in a suitable thermal chamber in which the temperature shall be variable over the applicable temperature range (see 3.8.5). The delay line shall be allowed to reach thermal stability at a sufficient number of temperatures covering the applicable temperature range (see 3.8.5) and at each stabilized temperature the delay time shall be measured and the delay time variation from the reference temperature delay time shall be recorded (see 3.8.5).

$$\text{ppm/°C} = \frac{\text{(total delay at 125°C) - (total delay at 25°C)}}{\text{(total delay at 25°C) (125°C - 25°C)}} 10^6$$

$$\text{ppm/°C} = \frac{\text{(total delay at -55°C) - (total delay at 25°C)}}{\text{(total delay at 25°C) [25°C - (-55°C)]}} 10^6$$

4.6.6.1.5.1 Alternate measuring method. The following alternate method for measuring delay time variation using pulse width may be used:

$$\Delta Td = \frac{\Delta PW \text{ at extreme temperature}}{2}$$

To convert Td to PPM/°C: Td (ns) at extreme temperature X 10^6 = PPM/°C.

4.6.6.1.6 DC resistance (see 3.8.6). Direct current (dc) resistance shall be measured in accordance with method 303 of MIL-STD-202.

4.6.6.1.7 Nominal characteristic impedance (at input) (see 3.8.7). Nominal characteristic impedance shall be measured with suitable equipment and shall conform to the values listed in applicable specification sheets (see 3.1).

4.6.6.1.8 Insulation resistance (see 3.8.8). The delay lines shall be subjected to the insulation resistance test outlined in method 302 of MIL-STD-202. The following details shall apply:

a. Test condition: A.

b. Measurements shall be taken between input and ground. Metal cases shall also be tested between terminals and case.

4.6.7 Resistance to solvents (see 3.9). Delay lines shall be tested in accordance with method 215 of MIL-STD-202.

4.6.8 Solderability (see 3.10). Delay lines shall be tested in accordance with method 208 of MIL-STD-202. The following details shall apply:

a. Special preparation of specimen: Sample units shall not have been soldered during any of the previous tests. Solder dipping in accordance with 3.4.5.1 is permitted.

b. All terminals of each part shall be tested.

4.6.9 Moisture resistance (see 3.11). Unless otherwise specified (see 3.1), delay lines shall be tested in accordance with method 106 of MIL-STD-202, except step 7b, which is not applicable. Load voltages are not applicable. Measurement before and after: Winding continuity in accordance with 3.21 and 4.6.19.

4.6.10 Salt spray (corrosion) (metal cases only) (see 3.12). Delay lines shall be tested in accordance with method 101 of MIL-STD-202, test condition A.

4.6.11 Vibration (see 3.13). Delay lines shall be tested in accordance with method 214 of MIL-STD-202. The following details shall apply:

a. Method of mounting: Delay lines shall be mounted by soldering to a printed wiring board.

b. One test point.

c. Test conditions I, K, 15 minutes.

d. Measurement before and after: Winding continuity in accordance with 3.21 and 4.6.19.

4.6.12 Shock (see 3.14). Unless otherwise specified (see 3.1), delay lines shall be tested in accordance with method 213 of MIL-STD-202, test condition I.

4.6.13 Life (see 3.15). Delay lines shall be tested in accordance with method 108 of MIL-STD-202. The following details shall apply:

a. Distance of temperature measurements from specimens: Three inches in still air.

b. Test temperature and tolerance: 125°C ±3°C (257°F ±5°F).

c. Operating conditions: Three volts, square wave, 50 percent duty cycle, output loaded with terminating impedance, taps not loaded, pulse width shall be three times the nominal total delay.

d. Test condition: D.

e. Measurements during test: Measure temperature daily. Measure total delay time at room temperature (within 2 hours of removal from elevated temperature) weekly. Add the time that the units are out of the 125°C environment to the total test time to ensure that test condition D is complied with.

f. Measurements after test: Electrical characteristics. Measure after units have returned to room temperature, but within 8 hours of the end of the life test.

4.6.14 Terminal strength (see 3.16). Delay lines shall be tested in accordance with method 211 of MIL-STD-202, test condition A, applied force 5 (+0.25/-0) pounds. One terminal on each test sample shall be subjected to the test.

4.6.15 Fungus (see 3.17). Unless certification is provided, delay lines shall be tested in accordance with method 508 of MIL-STD-810.

4.6.16 Dielectric withstanding voltage at reduced barometric pressure (see 3.18). Delay lines designed for operation above 10,000 feet shall be tested in accordance with method 105 of MIL-STD-202. The following details shall apply:

a. Duration of application of test voltage: Not less than 1 second, or more than 5 seconds. The duration of the test shall begin when 95 percent of the test potential is reached.

b. Points of application of test voltage: Between mutually insulated terminals. For metal cases, also test between terminals and case.

c. Limiting value of surge current: Shall not exceed 5 milliamperes (mA).

d. Test condition: C.

e. Magnitude of test voltage: 50 volts dc.

f. Examination during and after test: Delay lines shall be examined for evidence of arcing, flashover, breakdown of insulation, and damage.

4.6.17 Resistance to soldering heat (see 3.19). Delay lines shall be tested in accordance with method 210 of MIL-STD-202. The following details shall apply:

a. Special preparation of specimen: None.

b. Mount board shall not be metal clad.

c. Test condition: D.

d. Cooling time: Five minutes.

e. Examinations after test: Electrical characteristics and x-ray in two perpendicular planes (the two largest surface areas). The X-ray shall be performed by any means that will provide a clear contrast between the material density of the unit components. Three to ten power magnification shall be used to inspect for foreign material in the terminal area and for voids around the terminals.

4.6.18 Flammability (see 3.20). Delay lines shall be tested in accordance with method 111 of MIL-STD-202. The following details shall apply:

a. Point of flame application: The flame shall be applied to the body of each delay line.

b. Allowable time for burning of visible flame on specimen: Three minutes maximum.

c. Inspection during and after test: Delay lines shall be inspected for evidence of violent burning which results in an explosive-type fire, dripping or flaming material, and visible burning which continues beyond the allowable duration after removal of the applied flame.

4.6.19 Winding continuity (see 3.21). All windings of delay lines shall be tested for electrical continuity by any suitable means.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with the provisions specified for semiconductor devices in MIL-S-19491, level C, unless otherwise specified in the acquisition document.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Delay lines covered by this specification are designed to be used in electronic equipment where a pulse delay is required.

6.2 Acquisition data. The acquisition document should specify the following, as a minimum:

a. Title, number, and date of this specification.

b. Title, number, and date of the applicable specification sheet.

c. Complete military PIN (see 1.2.1 and 3.1).

d. Terminal finish code in accordance with MIL-STD-1276, revision B (see 3.4.5).

e. Packaging requirements, if other than those stated in 5.1.

6.3 Non-military drawings. Drawings describing non-military delay lines submitted to DESC for evaluation under the Military Parts Control Advisory Group (MPCAG) program should include, as a minimum, the following information:

a. Reference to MIL-D-83531 (when applicable).

b. Dimensions and tolerances.

c. Case and terminal materials.

d. Schematic (circuit diagram).

e. Operating temperature range.

f. Delay time (total).

g. Delay time (per tap).

h. Delay time variation with temperature.

i. Rise time.

j. Impedance (ohms).

k. Attenuation.

l. DC resistance.

m. Distortion.

n. Weight.

o. Part marking (index mark minimum).

p. Quality assurance provisions.

q. Vendor PIN.

r. Vendor CAGE number (formerly FSCM).

NOTE: Drawings covering off-the-shelf commercial parts should be classified as specification control drawings.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time set for opening of bids, qualified for inclusion in the applicable qualified products list, whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Government tested for qualification, in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. The activity responsible for the qualified products list is the 645 LOG/ES, Gentile AF Station, Dayton, OH 45444-5400; however, information pertaining to qualification of products may be obtained from the Defense Electronics Supply Center, ATTN: DESC-EQ, Dayton, OH 45444-5000.

6.4.1 Copies of "Provisions Governing Qualification". Copies of SD-6, "Provisions Governing Qualification", may be obtained from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.

6.5 Tin plated finishes. Pure tin plating is prohibited (see 3.4.5), since it may result in tin wisker growth. This could, in turn, cause shorts and intermittents, especially in low-power (5 mA and below) applications. For additional information, see ASTM B545.

6.6 New specification sheets. A new specification sheet may be requested by supplying the following:

a. A proposed specification sheet prepared in the same format as the existing specification sheets.

b. An explanation of the difference(s) between the proposal and the most similar existing specification sheet.

c. A list of military contracts or systems in which the proposed specification sheet part(s) have been or will be used.

This information should be forwarded to both 645 LOG/ES, Gentile AFS, Dayton, OH 45444-5400 and the Defense Electronics Supply Center, ATTN: DESC-EMM, Dayton, OH 45444-5270.

6.7 Subject term (key word listing).

Microcircuit

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX

PROCEDURE FOR QUALIFICATION INSPECTION

10. SCOPE

10.1 Statement of scope. This appendix contains the details of the quality assurance program which serves as the basis for qualification. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance only.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SUBMISSION

30.1 Sample.

30.1.1 Single-type submission. A sample consisting of 22 sample units of the specific delay line for which qualification is sought shall be submitted.

30.1.2 Combined-type submission. To obtain qualification for all parts on an individual specification sheet for which qualification is sought, samples for testing shall be selected on the following basis:

a. Eleven sample units of the lowest nominal characteristic impedance, total delay time, and maximum attenuation by impedance for which qualification is sought shall be submitted.

b. Eleven sample units of the highest nominal characteristic impedance, with the associated highest total delay time and maximum attenuation by impedance for which qualification is sought shall be submitted.

30.1.3 Information to be submitted to the qualifying activity. The following information, along with that required by 6.4, shall be submitted to the qualifying activity:

a. A program outlining compliance with this appendix.

b. A list of all part numbers for which qualification is desired.

c. Drawings covering the design of these items, including the components and materials used.

d. A sample of the in-process inspections performed for each device type for which qualification is requested.

e. Test results demonstrating that at least 22 delay lines of the specification sheet for which qualification is requested have met the requirements of the applicable screening tests of the qualification inspection requirements of table I.

f. A program describing compliance with the product assurance requirements specified in MIL-STD-790.

30.1.4 Listing on the QPL. Listing on the QPL shall be granted after approval of the information submitted by the manufacturer (see 30.1.3).

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 85

Review activities:
Air Force - 19, 99
DLA - ES

User activities:
Navy - AS, CG, MC, SH

Preparing activity:
Air Force - 85

Agent:
DLA - ES

(Project 5999-0292)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-D-83531A	2. DOCUMENT DATE (YYMMDD)

3. DOCUMENT TITLE
Delay Lines, Passive, General Specification For

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) (1) Commercial (2) AUTOVON (If applicable)	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME 645 LOG/ES	b. TELEPHONE (Include Area Code) (1) Commercial (513) 296-5530 (2) DSN 986-5530
c. ADDRESS (Include Zip Code) Gentile Station 1060 Hamilton Street Dayton, OH 45444-5400	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340